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1.Performing Floating-Point Accumulation on a Modern FPGA in Single and Double Precision

ABSTRACT

In this paper, we discuss the feasibility of a floating-point accumulator (FPACC) on modern high-end FPGA devices. We explore different implementation scenarios and propose new FPACC architectures for both single and double precision floating-point addends. The proposed strategies can be easily adapted to the implement a multiply-accumulator (FPMAC), with one or two rounding stages, in both single and double precision as well. All the aforementioned designs are characterized by high operating frequencies (ranging from 130 to 300 MHz) and moderate occupation area (from 300 to 800 slices) when implemented on the VC5VSX50T FPGA, an entry level Virtex 5 from Xilinx

2.Accelerating the Nonuniform Fast Fourier Transform Using FPGAs

ABSTRACT

We present an FPGA accelerator for the Non-uniform Fast Fourier Transform, which is a technique to reconstruct images from arbitrarily sampled data. We accelerate the compute-intensive interpolation step of the NuFFT Gridding algorithm by implementing it on an FPGA. In order to ensure efficient memory performance, we present a novel FPGA implementation for Geometric Tiling based sorting of the arbitrary samples. The convolution is then performed by a novel Data Translation architecture which is composed of a multi-port local memory, dynamic coordinate-generator and a plug-and-play kernel pipeline. Our implementation is in single-precision floating point and has been ported onto the BEE3 platform. Experimental results show that our FPGA implementation can generate fairly high performance without sacrificing flexibility for various data-sizes and kernel functions. We demonstrate up to 8X speedup and up to 27 times higher performance-per-watt over a comparable CPU implementation and up to 20% higher performance-per-watt when compared to a relevant GPU implementation

3.A methodology for "on-line" monitoring system in a welding process using FPGAs

ABSTRACT

This paper presents both the hardware implementation and the simulation of a Kahnan filter algorithm for detecting "on-line" discontinuities in a Tungsten Inert Gas (TIG) welding process, by using an infrared sensor. For the hardware implementation of the Kaiman filter a Field Programmable Gate Array (FPGA) with 32 bit floating point arithmetic was used. The data used for the simulation proposal were previously acquired through the infrared sensor and stored during an off-line test. Afterwards, the results from the off-line test were analyzed and compared against the results obtained using the "on-line" filter implemented in the hardware, which was described using the VHDL hardware description language. The results of the filter implemented in the FPGA were simulated using the ModelSim tool. Finally, both the estimative consumption and performance of the FPGA are also shown.

4. FPGA-based optimized architecture for face recognition using fixed point Householder algorithm

ABSTRACT

Eigen values evaluation is the fundamental part usually for real-time pattern recognition applications but computational intensive. Numerically calculated Eigen values based on floating point operations induce errors due to rounding and truncation effects, and the error increases further when fixed point operations are involved. On the other hand, fixed point operations are time efficient for hardware implementation. A technique has been devised to implement fixed point Householder (HH) on FPGA by developing a co-design architecture which allows efficient evaluation of Eigen values within acceptable error limits by adjusting binary bit position in fixed point operations. A relationship has been developed to define error bounds for HH on FPGA. The validity of the proposed system is demonstrated by comparing the fixed and floating point data using six different image resolutions. It is shown that the proposed architecture is 30% time efficient compared to a floating point system and .01% less error than floating point.

5. Analysis and Improvement of a Secure Proxy Signature Scheme

ABSTRACT

Recently, Hu-Bin and Jin Chenhui proposed a new strong proxy signature scheme based on elliptic curve crypto system. They claimed that it is secure and efficient. However, this paper shows that the proposed scheme is not correct and there are several mistakes in their scheme. As an improvement, this paper presents a novel strong proxy signature scheme which corrects the weakness of Hu-Bin and Jin Chenhui's scheme. The improved scheme also possesses all security properties for a strong proxy signature scheme. Compared with Hu-Bin and Jin Chenhui's scheme and other systems, the improved scheme needs much less computation overhead and communication cost. It can be applied to electronics commerce and mobile agent environment.

6. Design and FPGA implementation of modular multiplication methods using cellular automata

ABSTRACT

Cellular automata (CA) have been accepted as a good evolutionary computational model for the simulation of complex physical systems. They have been used for various applications, such as parallel processing computations and number theory. In this paper, we studied the applications of cellular automata for the modular multiplications; we proposed two new architectures of multipliers based on cellular automata over finite field $GF(2^m)$. Since they have regularity, modularity and concurrency, they are suitable for VLSI implementation. The proposed architectures can be easily implemented into the hardware design of crypto-coprocessors

7. An Efficient Design of Security Accelerator for IEEE 802.15.4 Wireless Sensor Networks

ABSTRACT

In this paper, we provide a low cost AES core for ZigBee devices which accelerates the computation of AES algorithms. Also, by embedding the AES core, we present an efficient architecture of security accelerator satisfying the IEEE 802.15.4 specifications. In our experiments, we observed that the AES core and the security accelerator use fewer logic gates and consume lower power than other architectures based on block-wide and folded ones

8.Pinpointing Cache Timing Attacks on AES

ABSTRACT

The paper analyzes cache based timing attacks on optimized codes for Advanced Encryption Standard (AES). The work justifies that timing based cache attacks create hits in the first and second rounds of AES, in a manner that the timing variations leak information of the key. To the best of our knowledge, the paper justifies for the first time that these attacks are unable to force hits in the third round and concludes that a similar third round cache timing attack does not work. The paper experimentally verifies that protecting only the first two AES rounds thwarts cache based timing attacks

9.A framework for tunneled traffic analysis

ABSTRACT

Research in traffic classification is reaching into ever more difficult areas. Traditional techniques such as header and payload inspection are not providing sufficient information due to usage of non-standard ports and encryption. Promising alternative methods have been proposed based on the statistical behaviour of traffic flows. Although these methods can achieve quite high accuracies in non-encrypted traffic flows, traffic identification of encrypted traffic flows is still in its early stages. We argue that the results to date for encrypted traffic cannot help a network device such as a firewall make any useful decision, nor are there any indications that this may be achieved in the future. We propose a novel approach to cope with encrypted peer to peer network layer tunnels which are a particular problem in schools, universities, and larger corporate networks. First statistical techniques are used to identify the protocols present, a process that may take in the order of seconds. Next, based on the protocols discovered, and enterprise policies, a network device is advised to block, band-limit, or allow the whole tunnel, or a range of packet sizes within that tunnel. Preliminary research has concluded that VoIP traffic can be successfully handled by this approach and that advise to a network device can be practically useful. Work continues to apply these techniques to other protocols and mixes of protocols within a peer to peer tunnels

10.A Huffman Codes Based Approach to Achieve Minimum Redundancy

ABSTRACT

In this paper we had introduced more tighter bounds by decreasing the redundancy of source letter. Previously the sharper bounds were found if the number of source letter was large and also provided the redundancy 'r' of any discrete memory less source satisfied $r \geq 1 - H(P_N)$, where P_N is the least likely source letter probability. But we decreased the redundancy of source letter (N) to four and five.

11.Evolutionary Optimization of Service Times in Interactive Voice Response Systems

ABSTRACT

A call center is a system used by companies to provide a number of services to customers, which may vary from providing simple information to gathering and dealing with complaints or more complex transactions. The design of this kind of system is an important task, since the trend is that companies and institutions choose call centers as the primary option for customer relationship management. This paper presents an evolutionary algorithm based on Dandelion encoding to obtain near-optimal service trees which represent the structure of the desired call center. We introduce several modifications to the original Dandelion encoding in order to adapt it to the specific problem of service tree design. Two search space size reduction procedures improve the performance of the algorithm. Systematic experiments have been tackled in order to show the performance of our approach: first, we tackle different synthetic instances, where we discuss and analyze several aspects of the proposed evolutionary algorithm, and second, we tackle a real application, the design of the call center of an Italian telecommunications company. In all the experiments carried out we compare our approach with a lower bound for the problem based on information theory, and also with the results of a Huffman algorithm we have used for reference

12. A unified architecture for efficient data and Non-Data Aided frequency estimation for FPGA implementation and application to satellite communications

ABSTRACT

Modern codes such as Turbo and LDPC codes operate at low signal-to-noise ratios, which makes carrier synchronization a challenging problem. Hence in many waveforms, some known symbols are inserted periodically into the data stream to achieve Data-Aided (DA) synchronization. However, these known symbols decrease the throughput of the transmissions. The data symbols which are unknown can also be used for synchronization, in which case it is known as Non-Data Aided (NDA) synchronization. In this paper, we present an efficient structure which is almost the same for both the DA and NDA methods, especially suitable for implementation on Field Programmable Gate Arrays (FPGA). We discuss the implementation complexity and trade-offs involved in the FPGA implementation of this structure. We illustrate its utility by applying it to a satellite communications waveform, popularly known as DVB-S2.

13. FPGA Implementation of High Performance LDPC Decoder Using Modified 2-Bit Min-Sum Algorithm

ABSTRACT

It has been more than 30 years that statistical learning theory (SLT) has been introduced in the field of machine learning. Its objective is to provide a framework for studying the problem of inference that is of gaining knowledge, making predictions, making decisions or constructing models from a set of data. Support Vector Machine, a method based on SLT, then emerged and becoming a widely accepted method for solving real-world problems. This paper overviews the pattern recognition techniques and describes the state of art in SVM in the field of pattern recognition.

14. Fault-Tolerance with Graceful Degradation in Quality: A Design Methodology and its Application to Digital Signal Processing Systems

ABSTRACT

The tremendous increase in device density of present day designs is accompanied by a corresponding increase in transistor failures (hard faults), posing a major challenge to current fault tolerant techniques and tools. We propose a novel "design-time" fault-tolerance methodology at architecture/circuit levels to improve the reliability of applications, where it is possible to classify computations into two categories- (i) those which contribute to quality degradation and, (ii) those which result in total system failure. The proposed scheme enhances system reliability by making appropriate trade-offs between area, output quality (signal to noise ratio or mean square error), and fault tolerance. This low-overhead generic methodology is suitable not only for scaled CMOS technologies, but is also applicable to future nanotechnologies (carbon nanotubes etc.) as well, where such defects are expected to be prevalent. We evaluated this technique on a widely used DSP system - Finite Impulse Response (FIR) filters (where minor degradation in quality can be tolerated). Results show that our technique achieves an improvement between 73.4%-450% (in terms of total system failure probability under iso-redundancy) compared to conventional fault tolerance techniques.

15.A real-time image denoising chip

ABSTRACT

In this paper, we present a real-time image denoising chip. For each pixel of the image under processing, our design uses a mask on it to determine whether it is likely being corrupted by impulse noise or not. After the noise detection, we reconstruct the noisy pixel by considering the possible edges existed in the mask. Particularly, our design removes the noise from corrupted images efficiently and requires no previous training. Extensive simulations demonstrate that the proposed method achieves excellent performance in quantitative evaluation and visual quality. Furthermore, the computational complexity of the proposed method is low and its memory requirement is small. An efficient VLSI architecture for this scheme is developed and it yields a processing rate of about 150 MHz by using TSMC 0.18μm technology.

16. Real-Time Video Filtering and Overlay Character Generation on FPGA

ABSTRACT

Real-time video processing is a rapidly evolving field with growing applications in science and engineering. Portable video processing systems require design which reduces the power, memory usage, and resource utilization while maintaining real-time operation. General system architecture for real-time video filtering and overlay character generation, based on a Field Programmable Gate Array (FPGA) is presented and evaluated. After initial configuration over the parallel port connection, the video codec dumps a stream of pixels in ITU-R BT.656 format, 8-bits per component with sync signals, using a sampling clock of 27 MHz. This stream is then fed to a series of filters, format conversion and overlay character generator. Finally, the Video Graphics Array (VGA) generator receives the pixel stream and displays it on a monitor. The implemented design includes filters of different functions and character generator with keyboard interface. The real-time of application like stock ticker and time display are also demonstrated. The VHDL codes for the architecture were synthesized using Xilinx ISE 10.1 and targeted for Xilinx Spartan3E FPGA. The results show that this design gives good performance with short processing time, low resource utilization, small power consumption and memory usage.

17. Characterization of randomness sources in ring oscillator-based true random number generators in FPGAs

ABSTRACT

The paper deals with the characterization of sources of randomness in true random number generators aimed at cryptographic applications implemented in Field Programmable Gate Arrays (FPGA). One of the most often used source of randomness in logic devices is the timing jitter present in clock signals, generated using ring oscillators (RO). In order to estimate the entropy of the generated random bit-stream, it is necessary to characterize the employed timing jitter. Using the simulation of the clock jitter injection into the gates of RO we show that the proportion of jitter from uncorrelated and correlated noise sources on the overall period jitter depends on the number of delay elements (inverters). We also propose a new and precise method of the jitter measurement outside the device based on the use of the differential device outputs in conjunction with a differential oscilloscope probe. The measured standard deviation of the clock

period is more than two times smaller than the one obtained using traditional methods. Employing the proposed measurement method we show that the jitter profile of the RO-generated clock and its sensitivity to global jitter sources (e. g. deterministic jitter) is strongly dependent on the architecture and topology of the oscillator.

18.A unified architecture for efficient data and Non-Data Aided frequency estimation for FPGA implementation and application to satellite communications

ABSTRACT

Modern codes such as Turbo and LDPC codes operate at low signal-to-noise ratios, which makes carrier synchronization a challenging problem. Hence in many waveforms, some known symbols are inserted periodically into the data stream to achieve Data-Aided (DA) synchronization. However, these known symbols decrease the throughput of the transmissions. The data symbols which are unknown can also be used for synchronization, in which case it is known as Non-Data Aided (NDA) synchronization. In this paper, we present an efficient structure which is almost the same for both the DA and NDA methods, especially suitable for implementation on Field Programmable Gate Arrays (FPGA). We discuss the implementation complexity and trade-offs involved in the FPGA implementation of this structure. We illustrate its utility by applying it a satellite communications waveform, popularly known as DVB-S2.

19.Wideband video transmission MIMO-OFDM platform using LLR-based adaptive hierarchical modulation

ABSTRACT

In this paper, we present a 4×4 MIMO-OFDM system for wideband video transmission. This video transmission system is modified from the DVB-T system by including the MIMO technique and a proposed LLR-based adaptive hierarchical modulation involving channel SNR and H.264/AVC packet priority. In the proposed system, Reed-Solomon encoder packet format, inner interleaver structure and pilot pattern are designed for the adaptive hierarchical modulation and the MIMO-OFDM transmission. The proposed system can transmit at least four H.264/AVC streams at the same time and possesses high noise tolerability. Finally, we also design and develop an FPGA platform to emulate its feasibility and the hardware capability. The FPGA system runs at

48MHz and achieves 20Mbps~40Mbps throughput in 2×2 MIMO-OFDM transmission scheme at 6MHz bandwidth.

20.Design and implementation of a low-complexity RAKE receiver and Channel Estimator for DS-UWB

ABSTRACT

In this paper, the design and implementation of a low complexity Direct Sequence Ultra-Wideband (DS-UWB) receiver subsystem which incorporates a **Channel Estimator** (CE) and a novel hybrid Partial/Selective (HPS) RAKE Receiver (RR) **using** maximal ratio combining (MRC) is presented. The proposed architecture demonstrates the tradeoff between energy capture, performance and receiver complexity by combining the benefits of both partial and selective RAKE receiver algorithms. We focus our work on a highly parallel, modular, synthesizable design which is based on **FPGA** technology and it is optimized for high performance.

21.Performance analysis of different DSP algorithms on advanced microcontroller and FPGA

ABSTRACT

Digital signal processing (DSP) algorithms are mostly implemented on special purpose digital signal processors. Recently, advanced hybrid microcontrollers and field programmable gate arrays (FPGAs) are also evolving as the suitable platforms for realizing DSP algorithms. This paper aims towards the analysis of performance of popular DSP algorithms on advanced microcontroller and FPGAs. A time complexity analysis for different **filter** structures like finite impulse response (FIR), infinite impulse response (**IIR**) and **adaptive filter using** least mean square (LMS) algorithm etc. has been studied for AVR ATmega64L microcontroller with respect to MC56F8013 digital signal controller. The same algorithms have also been realized on FPGAs and performances have also been analyzed. A comparison has been done on the hardware utilization of different FPGAs (Xilinx Spartan3e, Virtex2, and Virtex4) for different algorithms. Based on the performance analysis, finally, the architecture of a reconfigurable processor has been proposed with a view to exploit the advantages of all these platforms.

22.Distributed Amplify-and-Forward with Ring-TCM Codes

ABSTRACT

This paper proposes a new distributed Amplify-and-Forward (AF) scheme which is integrated with the Ring-Trellis Coded Modulation (TCM) codes in order to achieve both high spectral efficiency and large diversity gain. In the distributed AF scheme, more users cooperate with each other. Each user still uses half of its transmission freedom for relaying others' signal. However, different to the conventional AF scheme, each user further partitions its relay transmission into smaller divisions in order to help more users. As a result, for each user, the distributed AF scheme will have the same spectral efficiency as the conventional AF scheme, but creating more diverse transition paths and providing better diversity gain. In the scheme, output symbols are demultiplexed into several subframes, each of which will be relayed by a different user. As a result, each output symbol from a trellis transition branch can be relayed by a different user, assisting error-correction performance of the decoder. This distributed coding scheme is suitable for different wireless access systems, such as WiLAN and WiMAX systems. Our simulation results show that with the same spectral efficiency, the distributed coded AF scheme can significantly outperform the conventional coded AF scheme.

23.Design and optimization of Serial communication system interface module

ABSTRACT

Serial communication system has been widely used in data communications and control system because of less hardware resources, anti-jamming ability, and easy to implement features. A FPGA-based high performance Serial communication system interface module which includes full functions of UART16550 is designed and optimized based on the communication protocol and working principles in this paper. Various technologies are adopted during the design and optimization procedure, such as the three always block coding style, EDA optimization, circuit optimization, and so on. The frequency of the optimized design is up to 166MHz, and the power consumption is reduced to 0.147W by 63.9%. The test data at typical baud-rate of 115200 and the analyzed result by using Matlab are presented. The test results indicate that the optimized design can be communicated correctly and steadily.

24. Simple traffic light controller: A digital systems design project

ABSTRACT

In the past few years, laboratory exercises for our Digital Systems course were typically self contained. The lack of integration prevented students from fully realizing a complete digital system during the course of the class. The simple traffic light controller design project was introduced to alleviate this shortcoming and to ensure students gain experience in solving implementation and interfacing problems of a modern digital system. Students implement a fully functional traffic signal controller for a four-way intersection. The intersection is complete with sensors to detect the presence of vehicles waiting at or approaching the intersection. The project incorporates many concepts and components that are discussed in detail throughout the course. These include FPGAs, VHDL for modeling and synthesis, finite state machines, embedded microprocessors, memory interfaces, serial communication, and signal synchronization. A bottom-up with a partially specified design methodology is used to encourage students to use their breadth of knowledge and creativity. By the end of the project, students will have gained a better understanding of digital system design methodologies through hands-on experience.

25. The design and application of one kind of multi-channel high-speed serial data acquisition system

ABSTRACT

A multi-channel high-speed serial data acquisition system based on LVDS interface is introduced. In the system, the FPGA APA300 produced by ACTEL Company used to control the serial to parallel conversion and data caching of multi-channel high-speed serial data. Then the parallel data is collected by the data acquisition card. The system can adjust itself by the standard data source generated by itself. The principle of the system, function realization of FPGA, and logic design of the LVDS interface are expounded. The system has high data acquisition rate, high reliability and strong anti-interference capability.

26. FPGA-based multi-channel CRC generator implementation

ABSTRACT

This article mainly describes a way of designing a parallel and highly pipelined Cyclic Redundancy Code (CRC) generator. The design can handle five different channels at an input rate of 2Gbps each. The generated CRCs are compatible

with the 32-bit Ethernet standards. This circuit has been implemented with the chip EP2C35F672C6 of ALTERA using the properties of Galois Field. The synthesis results show that the design can meet the needs of high-speed data integrity check.

27. Multiple communication-domains design in FPGA-based Systems-on-Chip

ABSTRACT

The increasing complexity of modern digital devices demands for ever increasing communication requirements, and for an ever increasing heterogeneity of the target applications. Specifically, different communication domains may be implemented using the same chip area, for instance to allow multiple parallel applications to be loaded onto the device. A flexible, reliable yet performant communication infrastructure is hereby proposed, to ensure inter-domain communication and cooperation. A novel communication-centric design is proposed to easily integrate classical bus-based systems with Network-on-Chip architectures, taking directly into consideration the resource requirements of the target FPGA device.

28. Circular-buffered architecture for Cellular Neural Networks-based analog Viterbi decoder

ABSTRACT

The Cellular Neural Network (CNN) based analog Viterbi decoder with a circular-buffered architecture is proposed for decoding partial response maximum likelihood (PRML) signals. The Viterbi decoder is an error correcting method utilizing the dynamic programming which is an efficient algorithm for finding the optimal path with the identical local computation performed at each node. In the previous CNN-based analog Viterbi decoder, a circularly connected cylindrical structure was presented. In this paper, a multiplexer-based cellular 2D structure is presented in which positions of its decoding and output stages are fixed and a multiplexer which distributes input data sequence to appropriate CNN trellis stages is employed. The proposed CNN-based Viterbi decoder is simpler, requires less silicon area, higher speed and has better performance than the previous one. The principle of the new architecture is uncovered and its decoding performance is compared with that of the previous architecture in this paper.

29. Common architecture for decoding turbo and LDPC codes

ABSTRACT

Turbo codes and Low Density Parity Check (LDPC) codes have been shown to be practical codes that can approach Shannon capacity in several communication systems. In terms of performance and implementation complexity, LDPC codes and turbo codes are highly comparable, especially at coding rates around 1/2. In many recent wireless standards such as 3GPP LTE and WiMax, both turbo and LDPC codes have been recommended at the encoder. However, the **decoder** for turbo codes involves **trellises** and the BCJR algorithm, while the **decoder** for LDPC codes uses sparse graphs and the message passing algorithm. Therefore, in several implementations, a designer is forced to implement either the turbo **decoder** or the LDPC **decoder**. The main idea behind this work is to enable the implementation of both **decoders** using a common architecture. We view the constituent convolutional code in a turbo code as a block code, and construct a sparse parity check matrix for it. Then, the sparse matrix and the associated bipartite graph are used for decoding the convolutional code by soft message passing algorithms. Simulation results show a manageable degradation in performance with a reduction in complexity.

30. Hardware design for fast intermode decision and for residues generaton in a variable block size motion estimation compliant with the H.264/AVC video coding standard

ABSTRACT

H.264/AVC is the latest video coding standard. It reaches the highest compression rates when compared to previous standards. On the other hand, it has a high computational complexity mainly due to motion estimation and its mode decision. Considering the high **number** of calculations, hardware implementations become essential. Moreover, it is important try to find alternatives to simplify the H.264/AVC mode decision. Another desirable improvement is an efficient way to provide the residual blocks of motion estimation to the next encoding steps. Addressing hardware architectures, this work presents an architecture for fast inter mode decision and production of residual blocks. The variable block-size motion estimation architecture **used** is based on full search algorithm, SAD calculation, and it produces the 41 motion vectors within a macroblock. The architectures were described in VHDL and

mapped to a Xilinx **FPGA**. Considering the results, the architecture reaches real time for HDTV 720p at 41 fps.

31. Libor market model simulation on an FPGA parallel machine

ABSTRACT

In this paper, we present a high performance scalable **FPGA** design and implementation of an interest rate derivative pricing engine that targets on the cap pricing. The design consists of a Gaussian random number generator, based on the Mersenne Twister uniform random generator, and a Monte Carlo path generation engine which calculates the prices of an interest rate derivative based on the LIBOR market model. We implemented this design on the Maxwell **FPGA** supercomputer using up to 32 Xilinx XC4VFX100 **FPGA** nodes. We have also compared our **FPGA** hardware implementation with an equivalent optimized pure software implementation running on up to 32 2.8GHz Xeon processors with 1 GB RAM each. This showed our **FPGA** implementation to be 58× faster than the optimized software implementation, while being more than two orders of magnitude more **energy efficient**. These results scale linearly with the number of **FPGA** and Xeon processor nodes **used**.

32.A low-cost stand-alone real-time multi-channel frequency monitoring system

ABSTRACT

In this paper, an affordable sophisticated standalone real-time multi-channel analog signal Acquisition and Frequency Detection and/or Monitoring (A FREDOM) system is proposed. The A FREDOM is **used** to acquire multi-channel real-time analog signals. It also detects and monitors their frequencies. Any change in any channel frequency is reported. A proper action is taken place upon frequency change. The A FREDOM is hardware reconfigurable. Accordingly, it can be utilized in various real world applications especially in hazardous environments, or isolated areas, for remote architecture reconfiguration, while keeping the cost of the device low. The hardware implementation of the different processing functions of the device allows for high-speed processing without the need of expensive general purpose processors. The target technology of implementing the proposed design is the System on Chip via Field Programmable Gate Array (SoC-**FPGA**). Performance evaluation and cost comparisons are shown via simulation and experiments.

33. FPGA-based improvement of classical current tracking methods for high-frequency power converters

ABSTRACT

Embedded microprocessors require efficient supply management systems to optimize its power consumption and to enhance their calculation potentials. Typically, the modules performing this function are known as Voltage Regulator Modules (VRMs). It is widely adapted that current-programmed regulation techniques own leveraging skills in the control of this kind of power converters. However, these strategies require a fine inductor-current sensing to achieve accurate results. One critical issue in the inductor-current sensing is the effect of parasitic inductances in the measurement loop. This undesirable effect produces a considerable mismatch between the real inductor-current waveform and the equivalent voltage image captured thanks to the shunt resistance. Further, this unwanted deviation augments as long as the current value is increased. As a result, this problem makes loosely the data obtained. However, today's commercial digital controllers, like FPGAs¹, can be used to reduce overwhelmingly the aforementioned drawback. The presented work exploits some intrinsic advantages of FPGAs such as its great processing speed and its parallel working mode to overcome this drawback. Therefore, a new digital auto-tuning system is proposed in which this undesirable effect is treated and compensated. The obtained result is a digital signal which avoids the parasitic effect of the inductance in the measurement loop. In the last part of our work, some experimental results, using a FPGA, validate the advantages of the proposed method.

34. An FPGA based real-time remote temperature measurement system

ABSTRACT

This paper presents a wireless re-programmable real time temperature measurement system designed using the hardware description language and realized in hardware using the field programmable array (FPGA). The proposed system is able to measure the real time temperature of various remote locations with each of them to an accuracy of 0.25 °C. It uses wireless transmission with the data rate of 115Kbytes/s, to transmit the measured temperatures to the central control system for motioning purpose. In addition, the proposed system incorporates feature that controls the temperature at the remote locations in real time. This system effectively works for a distance of 60m between the temperature measurement locations and the control station. Since this proposed

system **uses** a re-programmable controller, it is possible to customize the design to various industry applications. This paper presents the simulation and experimental results of the proposed system.

35.Design of real-time small target detection system for infrared image based on FPGA

ABSTRACT

A simple detection measurement is developed for real-time small target detection in infrared background, which can be easily available on **FPGA**. Basing on the difference between target and background, a predictive background is generated via restraining the infrared background with median filter, and then global threshold segmentation is **used** to residual image for further processing. Taking advantage of the relationship of targets in frames, a comprehensive analysis of residual image is made, and then the precise position of target is got by removing pseudo-objectives. Experiment results show that the method is simple to apply to hardware system, improve the system's false alarm rate and meet the requirements of practical engineering.

36.FPGA based wide range optical sensor: Vibration detection of compressor blades in high speed turbine engines

ABSTRACT

Vibration in high speed turbine engines is a performance limiting factor. Optical sensors can be **used** to accurately measure vibration in high speed turbo machinery. This paper will overview the development of the hardware and software whose purpose is to quantify these vibrations and present this data in a easy to understand fashion to the end user.

37. A method of automatic people counting used in air-conditioning energy-saving

ABSTRACT

This paper proposes a method of automatic people counting **used** in air-conditioning **energy**-saving. The method has counted the number of people in the indoor environments through three modules: image pre-processing module, image marking module and people counting module, in order to control air-conditioning controller to achieve the purpose of saving **energy**. Through experiment comparing, image pre-processing module chooses image graying,

Gaussian average filter, binarization and opening operation to optimize images. The following image marking module **uses** connected component detection algorithm, removing false contouring based on head shape properties and region marking. Finally, people counting module is **used** to count the number of people. The experimental results show that the method of automatic people counting about a large number of indoor images is effective and can maintain high statistics accuracy to those images which have little background noise. The method is very suitable for small cost of air-conditioning system to realize air-conditioning **energy**-saving and achieve the goal of **energy** saving.

38. Solar energy storage using hydrogen technology

ABSTRACT

At present, photovoltaic (PV) power plants are the fastest-growing renewable **energy** source in the Czech Republic. This rapid development of PV sources is having a negative effect on the electric power system control. One option for mitigating this effect is to store the **energy** generated by PV in times of excess power in the grid and supply it to the grid when required, i.e., during peak periods of the daily load curve.

39.Using inductive method to teach nuclear energy

ABSTRACT

The author has been teaching a survey course on nuclear **energy** in the past several years with internet resources without textbooks. The resources are organized in a way to facility inductive learning but with available documents for deductive learners as well. The course has received good reviews from students as the topics are relevant and the teaching encourages deep learning.

40. Energy Use of biogas from waste water

ABSTRACT

Paper deals with **using** biogas produced by wastewater treatment plant for electricity production. In the first part technology of the biogas production in waste water treatment plant (WWTP) is described, and then production of electricity and bargain redemption price are discussed.

41.Saddle-Point Equilibrium of Dynamic Game for Bilinear System

ABSTRACT

In this paper, saddle point equilibrium **problem** of the bilinear **quadratic** performance index dynamic game will be discussed from the basic saddle point equilibrium strategy of the game theory, by introducing a proper transformation, transforming the bilinear systems of nonlinear two points boundary value **problem** into a "separation" form of the linear two-point boundary, and then finding the saddle-point iteration method **using** equilibrium strategies.

42. A Method for Lane Detection Based on Color Clustering

ABSTRACT

Concerning the **problem** of lane detection in the Lane Departure Warning (LDW) system, this paper presents one method to detect the region of lane marking based on the CIELab color features clustering. Color space can provide us more precious information than gray scale. This algorithm proves that it is feasible to recognize lane marking by **using** color clustering. According to the geometry feature of road, **quadratic** curve is adopted to match the lane. And also, least square method is proposed to depict the parameters of **quadratic** curve.

43.Self-repairing and tuning reconfigurable electronics for space

ABSTRACT

Space missions often require technologies not yet available for earth applications. This talk will present the development of self-reconfigurable electronics for two real-world **problems** met by NASA: extreme environment electronics and navigation grade miniaturized inertial measurement sensor. Radiation and extreme-temperature hardened electronics is needed to survive the harsh environments beyond earth's atmosphere. Traditional approaches to preserve electronics incorporate radiation shielding, insulation and redundancy at the expense of power and weight. This presentation will demonstrate the implementation of a self-adaptive system **using** a field programmable gate array (**FPGA**) and data converters which can autonomously recover the lost functionality of a reconfigurable analog array (RAA) integrated circuit (IC). The

second application is related to the development of inexpensive, navigation grade, miniaturized inertial measurement unit (IMU), which surpasses the current state-of-the art in performance, compactness (both size and mass) and power efficiency **used** by all NASA missions. The talk will explain a self-tuning method for reconfigurable Micro-Electro-Mechanical Systems (MEMS) gyroscopes based on evolutionary computation that has the capacity to efficiently increase the sensitivity of MEMS gyroscopes through in-situ tuning. Didier Keymeulen joined the computer science division of the Japanese National Electrotechnical Laboratory as senior researcher in 1996. In 1998 he moved to the Jet Propulsion Laboratory and is currently principal member of the technical staff in the Bio-Inspired Technologies Group. At JPL, he is responsible for the applications of the DoD and NASA projects on evolvable hardware for adaptive computing that lead to the development of fault-tolerant electronics and autonomous and adaptive sensor technologies. He is the electronics test lead of the tunable laser spectrum (TLS) instrument on the 2011 Mars Science Laboratory (MSL) rover mission- - to Mars. He served as chair, co-chair, and program-chair of the NASA/ESA Conference on Adaptive Hardware and Systems. Didier received his BSEE, MSEE and Ph.D. in Electrical Engineering and Computer Science from the Free University of Brussels, Belgium.

44. Scalable mean voter for fault-tolerant mixed-signal circuits

ABSTRACT

Redundancy techniques, such as N-tuple modular redundancy has been widely **used** to improve the reliability of digital circuits. Unfortunately nothing substantial has been done for the **analog** and mixed signal systems. In this paper, we propose a redundancy based fault-tolerant methodology to design a highly reliable **analog** and digital circuits and systems. The key contribution of our work is an innovative mean voter. This mean voter is a low power, small area, very high bandwidth and linearly scalable voting circuit. Unlike other conventional voters which works with odd N in an NMR, the mean voter works for both odd and even N for **analog** units and hence reduces the area and power further. For the proof of concept, we designed two fault tolerant **analog** circuits i.e. a low pass anti-aliasing **analog filter** and a 4-bit flash ADC. We also presented fault-tolerance mechanism in 4-bit binary adder and an **FPGA** cell for demonstrating its advantage in digital applications. Experimental results are reported to verify the concepts and measure the system's reliability when single upset transient may occur.

45.FPGA design for multi-filtering techniques using flag-bit and flicker clock

ABSTRACT

Real time systems typically suffer from delay in data processing. This delay is caused by many reasons such as computational power, processor unit architecture, and synchronization signals in these systems. In order to increase the processing power, a new architecture and clocking technique is carried out in this paper hence the performance. This new architecture design called Embedded Parallel Systolic **Filters** (EPSF) would process data gathered from sensors and landmarks **using** a high density **FPGA** chip. The results show that EPSF architecture and bit-flag with a flicker clock perform significantly better in multiple input sensors signals under both continuous and interrupted conditions. Unlike the usual processing units in previous tracking and navigation systems **used** in robots, this system allows autonomous control of the robot through multiple techniques of **filtering** and processing strategy. Furthermore, it also offer a speedy performance that minimizing the delay about 50%.

46.A digital correction technique for channel mismatch in TI $\Sigma\Delta$ ADCs

ABSTRACT

Time interleaved sigma-delta **analog** to digital converter seems to be a potential solution for wide bandwidth **analog** to digital converter with the lowest hardware complexity compared to other solutions **using** parallel sigma-delta modulators. Its performance depends on the digital **filter** and is very sensitive to the channel mismatch. This paper summarizes our work on the digital signal processing for this kind of converter, including **filtering**, decimation and channel mismatch correction in order to reduce the implementation complexity while minimizing the channel mismatch effect.

47. An FPGA-based architecture for linear and morphological image filtering

ABSTRACT

Field Programmable Gate Array (FPGA) technology has become a viable target for the implementation of real time algorithms suited to video image processing applications. The unique architecture of the FPGA has allowed the technology to be used in many applications encompassing all aspects of video image processing. Among those algorithms, linear filtering based on a 2D convolution, and non-linear 2D morphological filters, represent a basic set of image operations for a number of applications. In this work, an implementation of linear and morphological image filtering using a FPGA NexysII, Xilinx, Spartan 3E, with educational purposes, is presented. The system is connected to a USB port of a personal computer, which in that way form a powerful and low-cost design station. The FPGA-based system is accessed through a Matlab graphical user interface, which handles the communication setup. A comparison between results obtained from MATLAB simulations and the described FPGA-based implementation is presented.

48. The design of image edge detection system based on EDA technique

ABSTRACT

Principle of image edge detection system and advantages of FPGA technique in processing speed and exploitation period are discussed briefly and feasibility based on Sobel operator to implement image edge detection is analyzed. Coprocessor module of image edge detection with EDA+FPGA technique is presented to meet the real-time request of image edge detection. Synthesis and waveform simulation prove that the design of image edge detection system is correct.

49. Real-time calibration-free autonomous eye tracker

ABSTRACT

In several fields of medicine, transportation and security the instantaneous gaze direction of a person under supervision is of crucial importance. We developed a contactless stereoscopic video-based eye tracker which works without any individual calibration. In real time it delivers information about the gaze direction frame by frame. The introduced algorithms are designed for computing the gaze direction within image acquisition time that is only limited by the hardware setup. The cameras are integrated into front-end modules by means of FPGA (programmable logic) circuits for image processing. Computation of the gaze direction is based on the spatial position of the pupil which is detected by a five-dimensional Hough transform. The system works under ambient light conditions whereas additional infrared illumination can be used to become independent of ambient light.

50. Motion detection of vehicles based on FPGA

ABSTRACT

In this paper a hardware approach for evaluating motion detection of vehicles on transit roads was proposed. A motion detection method is used through computational vision with a fixed camera which is based on the difference between the current image and a reference image of the environment that is being monitored. Results are compared with a software approach in order to validate and show the effectiveness of a hardware approach. Experiments based on real vehicle images in roads were performed and results are 7.5 times faster by using a reconfigurable hardware approach as compared to the same application in a software approach. The results were also compared with another hardware approach for motion detection and a performance improvement of about 66% was observed in the image processing.

51. Iris Biometric Processor Enhanced Module FPGA-Based Design

ABSTRACT

Iris Identification is nowadays one of the most promising techniques in Authentication. Most modern iris recognition systems are currently deployed on traditional sequential digital systems, such as a simple DSPs or MIPS processor. However, in this method, we can only match each data one by one, which will waste much time. In this study, iris matching, a repeatedly executed portion of a modern iris recognition algorithm is parallelized on an FPGA system. We demonstrate a 22 times speedup of the parallelized algorithm on the FPGA system when compared to a simple DSPs.

52. Fault tolerance on interleaved inverter with magnetic couplers

BSTRACT

The paper focuses on a new control strategy for improving the availability of power electronic converters based on interleaved structures. By using this strategy, the power electronic converters can continue to work (with reduced output power) in case of power component failure. The paper describes how to adapt the magnetic output filtering structure for this original control strategy. This structure is based on a monolithic coupler or a coupling transformer. Which are usually employed to minimize in a significant way the mass of the converters. They are normally sized to work with a fixed number of phases. Our control strategy induces new constraints on magnetic component, especially saturation problems. To reduce this problem some extra switch are added. Finally an experimental Power electronic converter driven by an FPGA is presented with the experimental results. It shows some experimental results with a 6 phases converter who work with 5 or 4 phases, to simulate one or two converter leg breakdown.

53.A new quaternary FPGA based on a voltage-mode multi-valued circuit

ABSTRACT

FPGA structures are widely used due to early time-to-market and reduced non-recurring engineering costs in comparison to ASIC designs. Interconnections play a crucial role in modern FPGAs, because they dominate delay, power and area. Multiple-valued logic allows the reduction of the number of signals in the circuit, hence can serve as a mean to effectively curtail the impact of interconnections. In this work we propose a new FPGA structure based on a low-power quaternary voltage-mode device. The most important characteristics of the proposed architecture are the reduced fanout, low number of wires and switches, and the small wire length. We use a set of FIR filters as a demonstrator of the benefits of the quaternary representation in FPGAs. Results show a significant reduction on power consumption with small timing penalties.

54.Multi-output synchronously-rectified forward converter with load transient considered

ABSTRACT

In this paper, an FPGA-counter-based scheme is presented herein and applied to a forward converter with single isolation stage and multiple outputs having synchronous rectification (SR). With only the required comparators and without any analog-to-digital converter (ADC), the information on feedback output voltage is entirely obtained according to a counter. Therefore, the proposed control topology for an SR forward converter can improve the load transient response and the cross regulation. Besides, to further upgrade the load transient response, the proposed nonlinear control technique is applied. In this paper, the proposed control scheme is described and some experimental results are provided to verify its effectiveness.

55. An FPGA based real-time remote temperature measurement system

ABSTRACT

This paper presents a wireless re-programmable real time temperature measurement system designed using the hardware description language and realized in hardware using the field programmable array (FPGA). The proposed system is able to measure the real time temperature of various remote locations with each of them to an accuracy of 0.25 °C. It uses wireless transmission with the data rate of 115Kbytes/s, to transmit the measured temperatures to the central control system for motioning purpose. In addition, the proposed system incorporates feature that controls the temperature at the remote locations in real time. This system effectively works for a distance of 60m between the temperature measurement locations and the control station. Since this proposed system uses a re-programmable controller, it is possible to customize the design to various industry applications. This paper presents the simulation and experimental results of the proposed system.

56. Three-phase voltage doubler rectifier based on three-state switching cell for Uninterruptible Power Supply applications using FPGA

ABSTRACT

This paper presents a three-phase voltage doubler rectifier based on three-state switching cells for Uninterruptible Power Supply (UPS) applications using FPGA. Its main features are: high power factor, reduced conduction losses, weight and volume, simple control strategy based on One-cycle Control (OCC), and connection between input and output enabling the use of inverter and bypass. A theoretical analysis, simulation results and preliminaries experimental results from a 9 kW development stage lab model are presented.

57.FPGA-based spectral envelope preprocessor for power monitoring and control

ABSTRACT

Smart Grid and Smart Meter initiatives seek to enable energy providers and consumers to intelligently manage their energy needs through real-time monitoring, analysis, and control. We have developed an inexpensive **FPGA** implementation of a spectral envelope preprocessor. This **FPGA** permits cost-effective and richly detailed **power** consumption monitoring for individual loads or collections of loads. It permits a flexible trade-off between data transmission, storage, and computation requirements in a **power** monitoring or control system. The information from the **FPGA** can be used to coordinate the operation of **power electronic** controls.

58.Hardware efficient architectures of improved Jacobi method to solve the eigen problem

ABSTRACT

Eigenvalue computation is essential in many fields of science and engineering. For high performance and real-time applications, it needs to be carried out in hardware. This paper focuses on the exploration of an efficient hardware architecture which computes eigenvalues of symmetric matrices **based** on Jacobi method. The proposed architecture is more efficient than previous architectures reported in the literatures, mainly due to the use of the CORDIC algorithm and the improvement of the double rotation in Jacobi algorithm. The whole system has been carried out on **FPGA**'s by using the VHDL language, attempting to optimize the design